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EXAMINER	
PHU, PHUONG M	
ART UNIT	**PAPER NUMBER**
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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TH

Office Action Summary	Application No.	Applicant(s)	
	10/749,654	STASZEWSKI ET AL.	
	Examiner	Art Unit	
	Phuong Phu	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,12-18,20-22,24,25 and 32* is/are rejected.

7)☒ Claim(s) *6-11,19,23 and 26-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on 11/14/07. Accordingly, claims 1-32 are currently pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 32 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 32 recites the limitation "the receiver path comprises a history capacitor and a rotating capacitor". It is unclear in the claim whether the output of "history capacitor" is coupled to the input of the "rotating capacitor", or the output of " rotating capacitor" is coupled to the input of the " history capacitor", and similarly, it is unclear about the functional/operational/structural of input/output of the combination of "a history capacitor and a rotating capacitor" with the input/output "receiver path".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 12, 20, 21, 24 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Kenington (6,794,931), newly-cited.

-Regarding claim 1, Kenington discloses a integrated transceiver circuit (see figure 7, col. 1, lines 66-67, col. 7, line 48 to col. 6, line 10)), comprising:

a digital polar transmitter path (comprising (312)) that provides an amplitude/phase signal (outputted from (312) from a digital input "Message Input Signal(s), the transmitter path including at least one digital predistorter (316, 314) that predistorts the digital input to mitigate nonlinearities associated with a power amplifier (216) (see col. 5, line 48 to col. 6, line 10);

a receiver path (comprising (712)) associated with the digital transmitter path (see col. 5, line 50 to col. 6, line 4);

a coupling element (710) that provides the signal from the transmitter path to the receiver path (see col. 5, lines 51-53); and

a signal evaluator (718, 726) that determines values for at least one parameter associated with the digital predistorter based on the signal (see col. 5, line 51 to col. 6, line 10).

-Regarding claim 2, Kenington discloses that transmitter path comprises a process component (comprising (D/A, VCO), (considered here equivalent with the limitation "gain normalization component"), that transfers the digital input from a digitized signal domain, (considered here equivalent with the limitation "normalized domain", to a phase domain that is dependent on voltage variations inputted to (VCO) to generate a phase-modulated RF output of (VCO) (see col. 3, lines 56-62, col. 4, lines 47-55), (the voltage variations considered here equivalent with the limitation "(PVT) variations").

-Regarding claim 3, Kenington discloses that digital predistorter (316) preceding the gain normalization component on the transmitter path, such that the digital predistorter predistorts the digital input in the normalized domain (see figure 7).

-Regarding claim 12, Kenington discloses a transceiver circuit comprising elements shown in figure 7 except (216), (the transceiver circuit considered here equivalent with the limitation "integrated transceiver circuit"), and the power amplifier (216) external to the transceiver circuit, (the power amplifier considered here equivalent with the limitation "external power amplifier").

-Regarding claim 20, Kenington teaches that the invention is to provide more linear amplification of the linearity of the power amplifier (see col. 1, line 65-67), namely to provide restoration of the linearity of the power amplifier from the non-linearity (saturation) and maintenance the linearity. Therefore, it can be said here that in Kenington, transmitter path being operative to alternate between a saturation mode, in which the power amplifier is driven at saturation, and a linear mode, in which the power amplifier operates within a linear range.

-Regarding claim 21, as similarly applied to claims 1-3, 12 and 20 set forth above and herein incorporated, Kenington discloses a method (see figure 7) of calibrating a predistortion component in a transceiver system, comprising:

procedure (312) of providing a first digital signal to (314, 718), containing amplitude information related to a desired analog signal (RF OUTPUT), to a transmitter path (312, 216, 710);

procedure (312) of providing a second digital signal to (316, 726), containing phase information related to the desired analog signal, to the transmitter path;

procedure (314, 316) of predistorting at least one of the first digital signal and the second digital signal in the digital domain according to at least one predistortion parameter;

procedure (216) of generating an analog signal from the first digital signal and the second digital signal; and

procedure (comprising (710, 718, 726)) of processing the analog signal at a receiver path (comprising (710, 712)) associated with the transmitter path to determine values for the at least one predistortion parameter.

-Regarding claim 24, as similarly applied to claims 1-3, 12, 20 and 21 set forth above and herein incorporated, Kenington discloses a integrated transceiver circuit (see figure 7), comprising:

means (312) for producing a digital input to (316, 726);

means (316) for predistorting the digital input to mitigate nonlinear error associated with a power amplifier (216) according to one or more predistortion parameters;

means (D/A, VCO) for converting the digital input from a normalized domain to a (PVT) dependent domain;

means (comprising (VCO, 216)) for generating an analog signal from the digital input; and

means (comprising (726)) for analyzing the analog signal to determine appropriate predistortion parameters for the means for predistorting.

-Regarding claim 25, Kenington discloses means for generating the analog signal comprising means (VCO) for synthesizing a radio frequency signal from a digital input.

6. Claims 1 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by McCune et al (6,366,177), newly-cited.

-Regarding claim 1, McCune et al discloses an integrated transceiver circuit (see figure 10, col. 5, lines 3-65), comprising:

a digital polar transmitter path (1001, 1007) that provides a amplitude/phase signal (outputted from (1025a, 1025b)) from a digital input (1003), the transmitter path including at least one digital predistorter (1021, 1023, 1025a, 1025b, 1027, 1029) that predistorts the digital input to mitigate nonlinearities associated with a power amplifier (1007);

a receiver path (1031, 1033, 1011) associated with the digital transmitter path;

a coupling element (inherently included for splitting the output from (1007) to (1031, 1033) that provides the signal from the transmitter path to the receiver path; and

a signal evaluator (1031, 1033, 1011) that determines values for at least one parameter associated with the digital predistorter based on the signal.

-Regarding claim 12, McCune et al discloses that power amplifier comprising an external power amplifier (1007) that is external to the integrated transceiver circuit (being the circuit shown in figure 10 except (1007)).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenington.

-Regarding claim 4, Kenington discloses that power amplifier comprising an amplifier (High-Speed RF Switch, 216), (considered here equivalent with the limitation "internal power amplifier"), that is integrated into the integrated transceiver circuit (700), the power amplifier accepting a digital input (outputted from (219)) (see col. 3, line 62 to col. 4, line 23).

Kenington does not teach that the digital input is a digital RF input, as claimed

However, Kenington teaches that the digital input is a high-frequency digital signal to provide a high-speed switch of (RF Switch) (see col. 4, lines 13-23).

Implementing high-frequency digital signals at RF is within skills of those people in the art, and well-known in the art, and the examiner takes Official Notice.

Since Kenington requires the digital input with a high frequency, it would have been obvious for one skilled in the art to implement the digital input, as a digital RF signal, in order to obtain the digital input with a high frequency for the high-speed switch of the (RF Switch), as expected.

-Regarding claim 5, Kenington teaches that the power amplifier can be a Class E switching amplifier (see col. 1, lines 13-16).

9. Claims 1, 12, 13, 14, 15, 16, 18, 21, 22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Camp, Jr et al (6,191,653), newly-cited.

-Regarding claim 1, Camp, Jr et al discloses an integrated transceiver circuit (see figure 5, col. 3, line 8 to col. 4, line 38, col. 6, line 28 to col. 7, line 12), comprising:

a polar transmitter path (comprising (14, 30, 32)) that provides an amplitude signal (A(t)) being an input (A(t), the transmitter path including at least one predistorter (48, 34) that predistorts the input to mitigate nonlinearities associated with a power amplifier (30, 32);

a receiver path (comprising (42, 48)) associated with the transmitter path;

a coupling element (inherently included for splitting the output of (32) to (24) and 42)) that provides the signal from the transmitter path to the receiver path; and

a signal evaluator (48) that determines values for at least one parameter associated with the digital predistorter based on the signal.

Camp, Jr et al does not teach that the input (A(t)) is digital signal.

However, implementing a polar signal as a digital polar signal is within skilled of those in the art, and well-known in the art, and the examiner takes Official Notice.

Since Camp, Jr et al does not particularly specify the input signal is analog or digital, it would have been obvious for one skilled in the art to implement the input signal (A(t)) as digital signal outputted from (14, 22, 20) in order to obtain the input signal as expected.

Camp, Jr et al does not teach that the at least one predistorter is a digital predistorter, as claimed.

However, Camp, Jr et al teaches that circuit functions of the integrated transceiver circuit can be configurable in a digital fashion (see col. 3, lines 20-25).

Therefore, it would have been obvious for one skilled in the art to implement the at least one predistorter as a digital predistorter, as taught by Camp, Jr et al, in order to obtain the at least one predistorter as expected.

(With such those above implementation, in Camp, Jr et al, the polar transmitter path (comprising (14, 30, 32)) can be considered here equivalent with the limitation "digital polar transmitter path".)

-Regarding claim 12, Camp, Jr et al discloses that power amplifier comprising an external power amplifier (32) that is external to the integrated transceiver circuit (shown in figure 5) except (32).

-Regarding claim 13, Camp, Jr et al discloses that the power amplifier further comprising an internal power amplifier (30), the output of the internal power amplifier being provided to the external power amplifier (see figure 5).

-Regarding claim 14, Camp, Jr et al discloses that transmitter path comprising an amplitude modulated path comprising (14, 22, 34, 48, 36) that controls the supply to the external amplifier (32) according to a first digital input outputted from (44) or (22), and a phase modulated path comprising (14, 20, 26, 28) that provides a radio frequency input to the external power amplifier according to a second input ($\phi(t)$).

Camp, Jr et al does not teach that the second input (D(t)) is a digital signal, as claimed.

However, implementing a polar signal as a digital polar signal is within skilled of those in the art, and well-known in the art, and the examiner takes Official Notice.

Since Camp, Jr et al does not particularly specify the second input signal is analog or digital, it would have been obvious for one skilled in the art to implement the second input signal as digital signal outputted from (14, 20, 22) in order to obtain the second input signal as expected.

-Regarding claim 15, Camp, Jr et al discloses that phase modulated path comprising a digitally controlled oscillator (452, 458, 456, 450) (see figure 5).

-Regarding claim 16, Camp, Jr et al discloses that phase modulated path comprising a process component (470, 452, 458, 456, 450), (considered here equivalent with the limitation "gain normalization component"), that adjusts the second digital input for process, voltage and temperature (PVT) variations associated with the digitally controlled oscillator (see col. 6, line 36 to col. 7, line 12).

-Regarding claim 18, Camp, Jr et al discloses that the amplitude modulated path comprises a digital predistorter (44, 46, 48, 34) that adjusts the first digital input to mitigate nonlinearities associated with the power amplifier (see figure 5).

-Regarding claim 21, as similarly applied to claims 1, 12, 13, 14, 15, 16, 18 set forth above and herein incorporated, Camp, Jr et al teaches method (see figure 5) of calibrating a predistortion component in a transceiver system, comprising:

procedure (14, 22) of providing a first signal (A(t)), containing amplitude information related to a desired analog signal outputted from (32), to a transmitter path;

procedure (14, 20) of providing a second digital signal (D(t)), containing phase information related to the desired analog signal, to the transmitter path;

procedure (comprising (48, 34)) of predistorting at least one of the first signal and the digital signal according to at least one predistortion parameter;

procedure (32) of generating an analog signal from the first signal and the second signal; and

procedure (42, 48) of processing the analog signal at a receiver path associated with the transmitter path to determine values for the at least one predistortion parameter.

Camp, Jr et al does not teach that the first signal and second signal are digital, as claimed.

However, implementing polar signals as digital polar signals is within skilled of those in the art, and well-known in the art, and the examiner takes Official Notice.

Since Camp, Jr et al does not particularly specify the first and second input signal is analog or digital, it would have been obvious for one skilled in the art to implement the first and second signals as digital signals outputted from (14, 22, 20) in order to obtain the first and second signals as expected.

Camp, Jr et al does not teach the procedure of predicting is processed in a digital domain, as claimed.

However, Camp, Jr et al teaches that circuit functions of method can be configurable in a digital fashion (see col. 3, lines 20-25).

Therefore, it would have been obvious for one skilled in the art to implement the procedure of predistorting as a digital process, as taught by Camp, Jr et al, in order to obtain the predistortion as expected.

-Regarding claim 22, Camp, Jr et al teaches procedure which comprises process (470, 472, 452) of converting the second digital signal from associated normalized domain to (PVT) dependent domain, and process (48, 34) of converting the first digital signal from associated normalized domain to (PVT) dependent domain (see figure 5).

-Regarding claim 24, as similarly applied to claims 1, 12, 13, 14, 15, 16, 18, 21, 22 set forth above and herein incorporated, Camp, Jr et al teaches an integrated transceiver circuit (see figure 5), comprising:

means (14, 22) for producing an input (A(t));

means (48, 34) for predistorting the input to mitigate nonlinear error associated with a power amplifier (32) according to one or more predistortion parameters;

means (48, 34) for converting the input from a normalized domain to a (PVT) dependent domain;

means (32) for generating an analog signal from the digital input; and

means (48) for analyzing the analog signal to determine appropriate predistortion parameters for the means for predistorting.

Camp, Jr et al does not teach that the input is digital, as claimed.

However, implementing a polar signal as a digital polar signal is within skilled of those in the art, and well-known in the art, and the examiner takes Official Notice.

Since Camp, Jr et al does not particularly specify the input signal is analog or digital, it would have been obvious for one skilled in the art to implement the input signal as digital signal outputted from (14, 20, 22) in order to obtain the input signal as expected.

-Regarding claim 25, Camp, Jr et al discloses that means for generating the analog signal comprising means (472, 452, 30, 32) for synthesizing a radio frequency signal outputted from (32) from a digital input outputted from (472) (see figure 2).

10. Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCune et al (6,366,177).

–Regarding claim 14, McCune et al discloses a the digital transmitter path comprising an amplitude modulated path (1023, 1025a, 1027) that controls the supply to the external amplifier according to a first input being an amplitude signal outputted from (1021), and a phase modulated path (1023, 1025b, 1029) that provides a radio frequency input (outputted from (1029) to the external power amplifier according to a second input being a phase signal outputted from (1021) (see figure 10).

McCune et al does not teach that the first and second input signals are digital, as claimed.

However, McCune et al teaches that the first and second input signals are generated from a Polar Signal Map (1021) (see figure 10).

Implementing a Polar Signal Map as a digital device for outputting digital signals is within skills of those in the art and well-known in the art, and the examiner takes Official Notice.

Since McCune et al does not teach in detail how the Polar Signal Map (1021) is implemented, it would have been obvious for one skilled in the art to implement Polar Signal Map as a digital device for providing the first and second input signals being digital signals, so that the first and second input signals would be obtained as expected.

-Regarding claim 17, the phase modulated path comprising a digital predistorter (1023, 1025b, 1029) that adjusts the second digital input to mitigate nonlinearities associated with the power amplifier (see figure 10).

Allowable Subject Matter

11. Claims 6-11, 19, 23 and 26-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

12. Applicant's arguments filed on 11/14/07 have been fully considered. As results, the previous rejections have been withdrawn. Claims 6-11, 19, 23 and 26-31 are indicated allowable as set forth above. However, the rest of the pending claims are deemed not allowable because of reasons set forth above in this Office Action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (8:00 AM - 4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phuong Phu
Primary Examiner

Art Unit 2611

Phuong Phu
01/25/08

PHUONG PHU
PRIMARY EXAMINER